MOSFET DEVICES HAVING LINEAR TRANSFER CHARACTERISTICS WHEN OPERATING IN VELOCITY SATURATION MODE AND METHODS OF FORMING AND OPERATING SAME

FIELD OF THE INVENTION

The present invention relates to semiconductor switching devices, and more particularly to switching devices for power switching and power amplification applications.

BACKGROUND OF THE INVENTION

Power MOSFETs have typically been developed for applications requiring power switching and power amplification. For power switching applications, the commercially available devices are typically DMOSFETs and UMOSFETs. In these devices, one main objective is obtaining a low specific on-resistance to reduce power losses. In a power MOSFET, the gate electrode provides turn-on and turn-off control upon the application of an appropriate gate bias. For example, turn-on in an N-type enhancement MOSFET occurs when a conductive N-type inversion-layer channel (also referred to as "channel region") is formed in the P-type base region in response to the application of a positive gate bias. The inversion-layer channel electrically connects the N-type source and drain regions and allows for majority carrier conduction therebetween.

The power MOSFET's gate electrode is separated from the base region by an intervening insulating layer, typically silicon dioxide. Because the gate is insulated from the base region, little if any gate current is required to maintain the MOSFET in a conductive state or to switch the MOSFET from an on-state to an off-state or vice-versa. The gate current is kept small during switching because the gate forms a capacitor with the MOSFET's base region. Thus, only charging and discharging current ("displacement current") is required during switching. Because of the high input impedance associated with the insulated-gate electrode, minimal current demands are placed on the gate and the gate drive circuitry can be easily implemented. Moreover, because current conduction in the MOSFET occurs through majority carrier transport through an inversion-layer channel, the delay associated with the recombination and storage of excess minority carriers is not present. Accordingly, the switching speed of power MOSFETs can be made orders of magnitude faster than that of bipolar transistors. Unlike bipolar transistors, power MOSFETs can be designed to withstand high current densities and the application of high voltages for relatively long durations, without encountering the destructive failure mechanism known as "second breakdown". Power MOSFETs can also be easily paralleled, because the forward voltage drop across power MOSFETs increases with increasing temperature, thereby promoting an even current distribution in parallel connected devices.

DMOSFETs and UMOSFETs are more fully described in a textbook by B. J. Baliga entitled *Power Semiconductor Devices*, PWS Publishing Co. (ISBN 0-534-94098-6) (1995), the disclosure of which is hereby incorporated herein by reference. Chapter 7 of this textbook describes power MOSFETs at pages 335–425. Examples of silicon power MOSFETs including accumulation, inversion and extended trench FETs having trench gate electrodes extending into the N+ drain region are also disclosed in an article by T. Syau, P. Venkatraman and B. J. Baliga, entitled

Comparison of Ultralow Specific On-Resistance UMOSFET Structures: The ACCUFET, EXTFET, INVFET, and Conventional UMOSFETS, IEEE Transactions on Electron Devices, Vol. 41, No. 5, May (1994). As described by Syau et al., specific on-resistances in the range of 100–250 $\mu\Omega cm^2$ were experimentally demonstrated for devices capable of supporting a maximum of 25 volts. However, the performance of these devices was limited by the fact that the forward blocking voltage must be supported across the gate oxide at the bottom of the trench.

FIG. **1**, which is a reproduction of FIG. **1** (*d*) from the aforementioned Syau et al. article, discloses a conventional UMOSFET structure. In the blocking mode of operation, this UMOSFET supports most of the forward blocking voltage across the N-type drift layer which must be doped at relatively low levels to obtain a high maximum blocking voltage capability, however low doping levels typically increase the on-state series resistance. Based on these competing design requirements of high blocking voltage and low on-state resistance, a fundamental figure of merit for power devices has been derived which relates specific on-resistance ($R_{on,sp}$) to the maximum blocking voltage (BV). As explained at page 373 of the aforementioned textbook to B. J. Baliga, the ideal specific on-resistance for an N-type silicon drift region is given by the following relation:

$$R_{on,sp}=5.93\times10^{-9}(BV)^{2.5} \quad (1)$$

Thus, for a device with 60 volt blocking capability, the ideal specific on-resistance is 170 $\mu\Omega cm^2$. However, because of the additional resistance contribution from the channel, reported specific on-resistances for UMOSFETs are typically much higher. For example, a UMOSFET having a specific on-resistance of 730 $\mu\Omega cm^2$ is disclosed in an article by H. Chang, entitled *Numerical and Experimental Comparison of 60V Vertical Double-Diffused MOSFETs and MOSFETs With A Trench-Gate Structure*, Solid-State Electronics, Vol. 32, No. 3,pp. 247–251, (1989). However, in this device a lower-than-ideal uniform doping concentration in the drift region was required to compensate for the high concentration of field lines near the bottom corner of the trench when blocking high forward voltages. U.S. Pat. Nos. 5,637,989 and 5,742,076 and U.S. Application Ser. No. 08/906,916, filed Aug. 6, 1997, the disclosures of which are hereby incorporated herein by reference, also disclose popular power semiconductor devices having vertical current carrying capability.

In particular, U.S. Pat. No. 5,637,898 to Baliga discloses a preferred silicon field effect transistor which is commonly referred to as a graded-doped (GD) UMOSFET. As illustrated by FIG. **2**, which is a reproduction of FIG. **3** from the '898 patent, a unit cell **100** of an integrated power semiconductor device field effect transistor may have a width "W_c" of 1 μm and comprise a highly doped drain layer **114** of first conductivity type (e.g., N+) substrate, a drift layer **112** of first conductivity type having a linearly graded doping concentration therein, a relatively thin base layer **116** of second conductivity type (e.g., P-type) and a highly doped source layer **118** of first conductivity type (e.g., N+). The drift layer **112** may be formed by epitaxially growing an N-type in-situ doped monocrystalline silicon layer having a thickness of 4 μm on an N-type drain layer **114** having a thickness of 100 μm and a doping concentration of greater than 1×10^{18} cm^{-3} (e.g. 1×10^{19} cm^{-3}) therein. The drift layer **112** also has a linearly graded doping concentration therein with a maximum concentration of 3×10^{17} cm^{-3} at the N+/N junction with the drain layer **114**, and a minimum concentration of 1×10^{16} cm^{-3} beginning at a distance 3 μm from the